

PD2-MFS

PowerDAQ II Simultaneous-Sampling Multifunction Boards

- 4/8 single-ended or 4/8* differential A/D channels (*optional)
- 300 kS/s – 2 MS/s sampling rate
- 12-, 14-, 16-bit resolution; optional gains 1, 2, 5, 10
- Two 12-bit analog outputs; 32 digital I/O; three 16-bit counter/timers
- Simultaneous operation of all subsystems
- Stream-to-disk capability
- Multiple boards operate in one PC
- Optional differential inputs
- Extensive triggering for A/D and D/A
- Full PCI-bus implementation



(PD2-MFS-8-1M/12 Shown)

Supports **UEIDAQ Framework** Data Acquisition Software Library for Windows, Linux and QNX drivers available. Visit our website for more details.

General Description:

For some applications, it's essential to sample several channels at the same time within a few nanoseconds—a feat not possible with multiplexed multi-channel boards no matter how fast their burst rate across all the channels. For these tasks, UEI is proud to offer the PD2-MFS Series, the only PCI boards currently available with as many as eight sample/hold amplifiers. This approach eliminates the need for expensive, bulky external simultaneous-sampling units. Not only do they offer the best in simultaneous sampling, they also come with the MF Series' array of other I/O capabilities including analog outputs, digital I/O and counter/timers.

PD2-MFS boards build on all the power of the PD2-MF Series including DSP control of all I/O subsystems. Here you have a choice of four or eight inputs running in either single-ended or differential modes. Three resolution grades and corresponding sampling rates are available: 16 bits (300 or 500 kS/s), 14 bits (500 kS/s, 800 kS/s and 2 MS/s) or 12 bits (1 MS/s). In addition, you can purchase models with individual per-channel programmable-gain amplifiers.

Specifications: (PD2-MFS-all models)

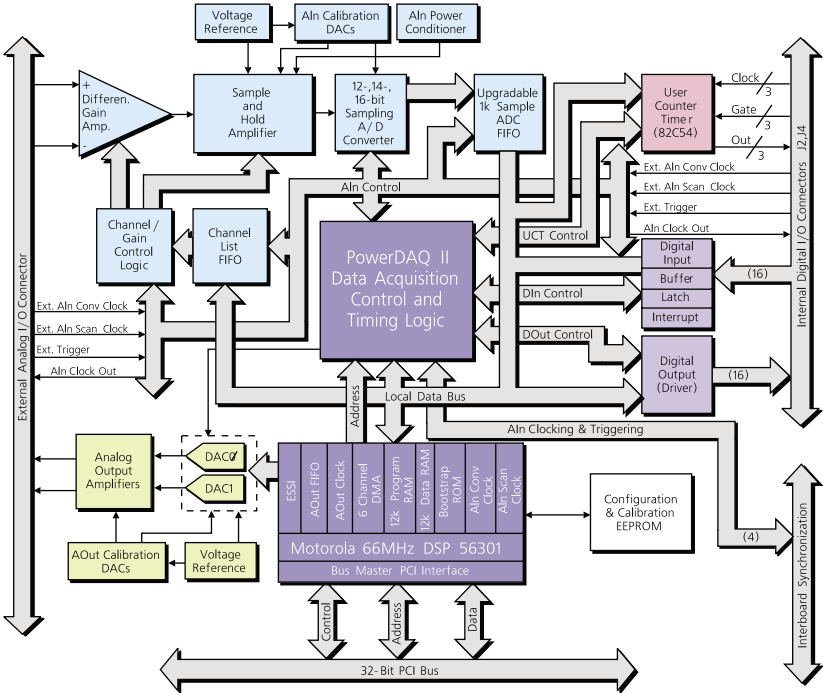
Digital I/O	
Input Bits (8 can generate IRQ)	16
Output Bits	16
Inputs	
High-level Input Voltage	2.0 V (min)
Low-level Input Voltage	0.8 V (max)
High-level Input Current	20 μ A
Low-level Input Current	-20 μ A
Outputs	
Output Driver High Voltage	2.5 V min, 3.0 V typ
Output Driver Low voltage:	(IOH = -32 mA) 0.55V max (IOL = 64 mA)
Current Sink	-32/64 mA max, 250 mA per port
Pulse Width	20 ns min, interrupt bit latched on rising, falling or either edge
Power-on Voltage	Logic Zero
Counter/Timer	
Number of channels	3 available to user (Intel 82C54)
Resolution	16 bits on each counter
Clock Inputs Software configurable	Internal 1 MS/s, External \leq 10 MS/s
High-level Input voltage	2.0V min
Low-level Input voltage	0.8V max
High-level Input current	20 μ A
Low-level Input current	-20 μ A
Gate Inputs	
Maximum Pulse Width	100 ns (High) 100 ns (Low)
Counter Outputs	Inverted
Output Driver High Voltage	2.5V min (IOH = 24 mA)
Output Driver Low Voltage	0.55V max (I _{OH} = 48 mA)

Analog Outputs	
Number of channels	2
Resolution	12 bits
Update Rate	200 kS/s each
Onboard FIFO Size	2k samples (on DSP)
Analog Output Range	\pm 10 V
Error	
Gain	\pm LSB
Zero	Calibrated to 0
Current Output	\pm 20 mA max
Output Impedance	0.3 Ω typ
Capacitive Drive Capability	1000 pF
Nonlinearity	\pm 1 LSB
Protection	Short circuit to analog ground
Power-on Voltage	0V \pm 10 mV
Setting Time to 0.01% of FSR	10 μ s, 20V step 1 μ s, 100-mV step
Slew Rate	30 V/ μ s
General Specifications	
Number of channels	5V
Resolution	10.5 x 3.8 (262 x 98 mm)
Environmental	
Operating Temperature Range	0 to 70°C
Storage Temperature Range	-25 to 85°C
Relative Humidity	to 95%, noncondensing
Connector J1	96-pin high-density Fujitsu connector (male) (Fujitsu PN#FCN-245P096-G/U)
Connector J2	36-pin header connector (male) (Thomas and Betts PN#609-3627)
Connector J4	36-pin header connector (male) (Thomas and Betts PN#609-3627)
Connector J6	8-pin male connector (Adam-Tech PN#PH2-SMT-8-SGA)

Technical Specifications:

Model: PD2-MFS-xx-	2M/14	1M/12	800/14	500/16	500/14	300/16
Resolution	14 bits	12 bits	14 bits	16 bits	14 bits	16 bits
Number of Channels Single-Ended Differential				4 (8 optional) 4 (8 optional)		
Maximum Sampling Rate (multiple channels)	2 MS/s	1 MS/s	800 kS/s	500 kS/s	500 kS/s	300 kS/s
Onboard FIFO Size (upgradeable to 16k, 32k, 64k)	4k samples			1k samples		
Input Ranges	0-5 V, ± 5 V, 0-8 V, ± 8 V @ 10 V ranges	0-5 V, 0-10 V ± 5 V, ± 10 V (software selectable)				
Channel-Gain List	256 entries					
Programmable Gains (by channel)	G=1 (or 1, 2, 5, 10 with -DG option)					
Drift Zero Gain	± 30 μ V/ $^{\circ}$ C ± 30 ppm/ $^{\circ}$ C					
Input Impedance	1 M Ω					
Input Bias Current	± 100 pA					
Input Overvoltage	± 18 V SE ± 40 V DI					
A/D Conversion Time	0.45 μ s	0.8 μ s	1.25 μ s	2.0 μ s	2.0 μ s	3 μ s
SSH Amp Settling Time	0.7 μ s	0.9 μ s	1.0 μ s	1.2 μ s	1.2 μ s	1.2 μ s
A/D Settling Time	0.4 μ s	0.6 μ s	1.25 μ s	1.5 μ s	1.2 μ s	2.7 μ s
DC Accuracy						
Nonlinearity (no missing codes)	± 2 LSB	± 0.5 LSB	± 0.5 LSB	± 1 LSB	± 1 LSB	± 1 LSB
AC Accuracy						
Effective Number of Bits	12.1	11.3	12.7	13.8	12.7	13.8
Channel Crosstalk	-80 dB @ 1 kS/s					
Clocking and Trigger Input						
Maximum A/D Pacer Clock	1500 kS/s @ 4 ch, 1700 kS/s @ 8 ch	975 kS/s @ 4 ch, 1095 kS/s @ 8 ch	800 kS/s	500 kS/s	500 kS/s	300 kS/s
External A/D Sample Clock Maximum Frequency	1500 kS/s @ 4 ch, 1700 kS/s @ 8 ch	975 kS/s @ 4 ch, 1095 kS/s @ 8 ch	800 kS/s	500 kS/s	500 kS/s	300 kS/s
Minimum Pulse Width	20 ns					
External Digital (TTL) Trigger High-level Input Voltage Low-level Input Voltage Minimum Pulse Width	2.0V min 0.8V min 20 ns					

Block Diagram:



Pinout Diagrams:

